In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 1-3 without prejudice.

1-3 (Cancelled)

4. (New) A computer system comprising:

a central processing unit (CPU) having:

a CPU core;

cache memory having a plurality of cache lines, each of the plurality of cache lines being compressible to form compressed cache lines to store additional data; and

compression/decompression logic; and

a memory controller coupled to the CPU having a compression map to indicate whether a cache line corresponding to a block of data in a system memory is in a compressed format.

5. (New) The computer system of claim 4 wherein the compression map includes bits that provides status for each aligned block in the system memory.

6. (New) The computer system of claim 4 wherein the compression/decompression logic compresses cache line data with a companion cache line as the data is passed from the CPU core to the cache memory.

7. (New) The computer system of claim 4 wherein the compression/decompression logic compresses cache line data with a companion cache line prior to the data being passed to the system memory.

8. (New) The computer system of claim 4 wherein the compression/decompression logic compresses cache line data with a companion cache line prior to the data being passed to a second CPU.

9. (New) The computer system of claim 4 wherein CPU further comprises a buffer to temporarily store cache line data prior to the data being compressed at the compression/decompression logic.

10. (New) The computer system of claim 4 further comprising:

a first interface to communicate with components that transmit and receive uncompressed cache line data; and

a second interface to communicate with components that transmit and receive compressed cache line data.

11. (New) The computer system of claim 4 further comprising cache coherency logic.

12. (New) A method comprising:

compressing one or more of a plurality of cache lines to form one or more compressed cache lines; and

updating a compression map a within a memory controller to indicate the one or more cache lines corresponding to a block of data in a system memory are in a compressed format.

13. (New) The method of claim 12 further comprising storing the compressed cache lines in a cache memory.

14. (New) The method of claim 12 wherein updating the compression map comprises updating a status bit associated with the block of data.

15. (New) The method of claim 12 further comprising buffering data corresponding to the cache lines prior to compressing the cache lines.

16. (New) The method of claim 13 further comprising transmitting the compressed cache lines to the system memory.

17. (New) A central processing unit (CPU) comprising:

a CPU core;

a cache memory having a plurality of cache lines, each of the plurality of cache lines being compressible to form compressed cache lines to store additional data;

compression/decompression logic; and

a memory controller having a compression map to indicate whether a cache line corresponding to a block of data in a system memory is in a compressed format.

18. (New) The CPU of claim 17 wherein the compression map includes bits that provides status for each aligned block in the system memory.

19. (New) The CPU of claim 17 wherein the compression/decompression logic compresses cache line data with a companion cache line as the data is passed from the CPU core to the cache memory.

20. (New) The CPU of claim 17 wherein the compression/decompression logic compresses cache line data with a companion cache line prior to the data being passed to the system memory.

21. (New) The CPU of claim 17 wherein the compression/decompression logic compresses cache line data with a companion cache line prior to the data being passed to a second CPU.

22. (New) The CPU of claim 17 wherein CPU further comprises a buffer to temporarily store cache line data prior to the data being compressed at the compression/decompression logic.

23. (New) The CPU of claim 17 further comprising:

a first interface to communicate with components that transmit and receive uncompressed cache line data; and

a second interface to communicate with components that transmit and receive compressed cache line data.